



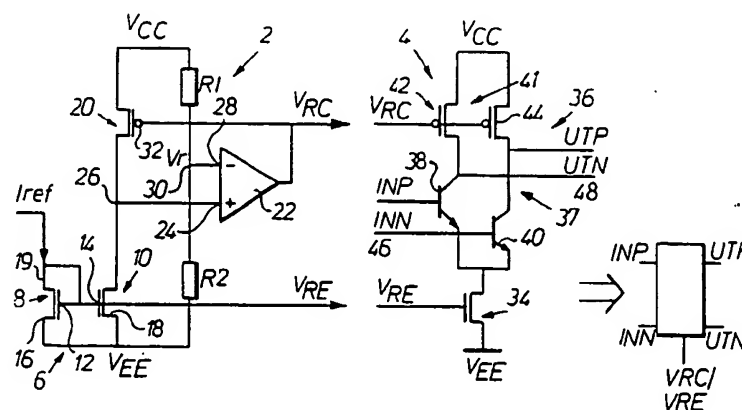
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(21) International Application Number: PCT/SE93/00520 (22) International Filing Date: 10 June 1993 (10.06.93) (30) Priority data: 9202033-8 1 July 1992 (01.07.92) SE (71) Applicant: TELEFONAKTIEBOLAGET LM ERICSSON [SE/SE]; S-126 25 Stockholm (SE). (72) Inventor: HEDBERG, Mats, Olof, Joakim ; Kvickrotsvägen 22, S-126 72 Haninge (SE). (74) Agents: DELHAGE, Einar et al.; Bergenstråhle & Lindvall AB, Box 17704, S-118 93 Stockholm (SE).		(81) Designated States: AU, BR, FI, KR, NO, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published With international search report.

(54) Title: A CONTROL CIRCUIT SYSTEM FOR CONTROL OF PARAMETERS IN LOGIC CIRCUITS OR SIMILAR



(57) Abstract

The invention relates to a control circuit system for controlling one or more parameters in a circuit with at least one operational stage (4), in the form of a delay stage or a logic stage, said operational stage comprising at least one operational circuit (37), at least one operational current source (34) for supplying a drive current for said operational stage, and at least one operational load (41). The operational stage comprises further a number of controllable components (34 and 42, 44) of said operational current source (34) and of said operational load (41), admitting control of the size of the drive current and of the load, respectively, in said operational stage. At least one reference stage (2) includes essentially an image circuit (10, 20) of said operational stage (4) with a reference current source (10) for supplying a drive current for said reference stage and a reference load (20), comprising a number of controllable reference components (10 and 20), admitting control of the size of the drive current and the load, respectively, of the reference stage. The reference stage, by means of a reference quantity (I_{ref}) controls the currents of said reference and operational current sources (10 and 34) to said reference load (20) and said operational load components (42, 44), respectively.

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A control circuit system for control of parameters
in logic circuits or similar.

5

Technical area

The present invention relates to a control circuit system for controlling one or more parameters in a circuit with at least one operational stage, particularly a differential stage, in the form of delay stage or a logic stage, said operational stage including

at least one operational circuit, at least one operational current source for supplying a first drive current to said operational stage, and at least one operational load.

The conception control includes here optimization and the conception parameter includes power and/or bandwidth and/or delay.

The state of the art

Power optimization and/or bandwidth optimization of logic circuits up to now has been obtained by designing different logic parts with different bandwidth, to enable optimization of bandwidth and by this reduction of power consumption.

As regards delay stages the state of the art includes different possibilities.

The most usual way is to adjust a threshold level or a decision point along a flank and thereby shift a switch-over of a following stage forwards or backwards in time.

Another method is to add or subtract a capacitive load in a circuit stage for coarse adjustment and change the current for fine adjustment.

A third method is to use diodes as collector loads. By varying the current through the diodes the resistances of these will vary, which in turn changes the time constants of

the circuit.

Description of the invention

5 The object of the invention is to provide a control circuit system, which enables control of the bandwidth of various delay and logic circuits in a controlled way.

This object is achieved by a control circuit system of the kind defined by way of introduction comprising

10 a number of first controllable current source and load components of said operational current source and said operational load for admitting control of the magnitude of said first drive current and of said operational load, respectively,

15 at least one reference stage comprising essentially an image circuit of said operational stage with

a reference current source for supplying a second drive current for said reference stage, and a reference load, said reference current source and said reference load comprising a number of second controllable current source and load
20 components for admitting control of the magnitude of said second drive current and of said reference load, respectively, and being essentially identical to said first current source and load components, respectively, said reference stage also including

25 an input stage connected for receiving an adjustable reference parameter and for controlling, by means of said reference parameter, current supply from said reference current source and said operational current source to said second and first controllable load components, respectively,

30 a comparison and control circuit connected for comparing the magnitude of said reference load with a load reference and for controlling an operational parameter of said reference load components and operational load components so as to keep the relationship between said reference load and

said load reference the same irrespective of the magnitude of the current through said reference load, and thereby keep the operational point of said operational stage constant for various drive currents in the latter.

5 The system according to the invention fulfils a requirement of being able to control the bandwidth, i.e. the speed, of various logic circuits and delay stages in a controlled manner. Of a number of different applications of a control circuit system according to the invention the
10 following can be mentioned:

- Delay line for e.g. data or clock signals.
- Oscillators where a delay stage determines the feedback time and by this the frequency
- Filter with controllable parameters
- 15 - Power optimization of logic circuits. Because the drive current is directly proportional to the bandwidth it is possible to design circuits which can be adapted to various speeds. By this it is possible to save power at lower speeds, based upon the understanding that unnecessary fast logic is
20 not necessary.

According to a preferred embodiment of the invention said reference parameter is a reference current and said input stage includes a transistor component connected for throughflow of said reference current, and said reference and
25 operational current sources include each an essentially identical transistor component, the control electrodes of which being connected to a voltage outlet of said transistor component of said input stage.

Said transistor components of said input stage and said
30 reference current source may be preferably interconnected in a current image circuit.

The load components of said reference stage and said operational stage are preferably transistor components, having control electrodes to which a voltage output from said

comparison and control circuit is connected.

Said comparison and control circuit may then include an operational amplifier having a first input connected for sensing the voltage over said load transistor component of said reference stage and a second input connected for sensing
5 a fixed reference voltage constituting said load reference.

Preferably said transistor components of said reference and operational current sources may be NMOS-transistors and said transistor components of said reference and operational
10 loads may be PMOS-transistors.

The control circuit system according to the invention can further comprise a number of reference stages, loads and current sources of the operational stage can be of different size than corresponding elements of the reference stage, and
15 the operational stage can include various combinations and numbers of operational stage, operational current source and operational load.

20 Descriptions of the Figures

The invention will now be described in detail with reference to the shown embodiments on the enclosed drawings, where

Figure 1 shows a circuit diagram of one embodiment of the control circuit system according to the invention,
25

Figure 2 shows a circuit diagram of a further embodiment of the control circuit system according to the invention,

Figure 3 shows a circuit diagram of a current controlled oscillator, which schematically illustrates an application of the invention for frequency control of a feedback delay stage
30 chain, and

Figure 4 shows a circuit diagram, which schematically illustrates an application of the invention in a mixed logic.

Preferred embodiments

In Figure 1 a reference stage is generally designated 2, and a logic stage or a simple delay stage is generally designated 4. To the right of the stage 4 the same is also shown symbolized as a delay stage. The task of the reference stage 2 is, as described in detail below, to keep the operational point of the logic stage/delay stage 4 constant for various drive currents.

The reference stage 2 as an input has a current image circuit, generally designated 6, which can be of a conventional design per se. More specifically, the current image circuit 6 includes two NMOS-transistors 8 and 10, which are arranged with their respective control electrodes 12 and 14 interconnected, and with their respective emitter electrodes 16 and 18 connected to a minimum voltage V_{EE} of the reference stage 2 and the logic stage 4. The collector electrode 19 of the transistor 8 is connected for receiving a reference current I_{ref} and interconnected with the control electrodes 12 and 14. Due to the current I_{ref} flowing through the transistor 8 a voltage V_{RE} caused by the resistance of the transistor 10 appears on the control electrode 12 of the transistor 8 as well as on the control electrode 14 of the transistor 10. For the transistor 10 the conception "reference current source" is here introduced for reasons, which will become apparent from the description below.

The transistor 10 in series with a PMOS-transistor 20 is connected in parallel with two resistances R1 and R2 between the voltage V_{EE} and a maximum voltage V_{CC} . The PMOS-transistor 20 constitutes a collector load of the NMOS-transistor 10. An operational amplifier 22 has a plus-input 24 connected to a voltage outlet 26 between the transistors 10 and 20, and a minus-input 28 connected to a voltage outlet 30. The output of the operational amplifier 22 is connected to the control electrode 32 of the PMOS-transistor 20 and has

a voltage designated V_{RC} . For the transistor 20 the conception "reference load" is here introduced for reasons which will become apparent from the further description below.

5 Between the voltage points V_{EE} and V_{CC} the logic stage 4 has an NMOS transistor 34 identical with the transistors 8 and 10 and a collector load, generally designated 36, of the transistor 34. The collector load 36 on the one hand includes an operational stage generally designated 37, comprising a
10 differentially connected stage of two transistors 38 and 40, and on the other hand an operational load generally designated 41. The operational load 41 comprises two PMOS-transistors 42 and 44, which constitute a collector load of the transistors 38 and 40, respectively. The transistors 42
15 and 44 are identical to the PMOS-transistor 20. On the respective control electrodes the transistor 34 is controlled by the voltage V_{RE} and the transistors 42 and 44 by the voltage V_{RC} . The inputs INP and INN, at 46, of the operational stage 37 are connected to the base electrodes of tran-
20 sistors 38 and 40, respectively, and their outputs UTP and UTN, at 48, are connected to the respective collector electrodes of the same transistors.

The way of operation of the described circuits is as follows.

25 The task of the reference stage 2 is to keep the operating point of the logic stage 4 constant for different drive currents. The reference stage 2 is an image circuit of the logic stage, and its PMOS- and NMOS-transistors have the same dimensional values as those in the logic, or are
30 specifically related thereto. The reference current I_{ref} is reflected partly to the PMOS-transistor 20 in the reference stage and partly to all controlled logic circuitry via the voltage reference V_{RE} . By this all controlled current sources work with the same reference.

To keep the output signal from the logic circuitry at 48 constant and independent of the collector resistance, it is necessary to adjust the collector load 42/44 in response to the current received from the current source 34, which is done by the reference stage 2. The reference stage has an internal voltage reference in the form of the voltage divider $R1/R2$ with the reference voltage V_r . This voltage is compared by the operational amplifier 22 with the voltage over the collector load 20. By means of the operational amplifier 22 the resistance of the collector load 20 is adjusted so as to keep the voltage drop over the latter similar to that over the resistance $R1$ irrespective of the magnitude of the current drawn through the transistor 20. The control voltage V_{RC} on the load 20 is distributed to all controlled logic, whereby all collector loads of the reference stage and the logic stage become equal. Since the swing over the collector load is small the load can be considered as purely resistive.

The voltage/time derivative of the output signal from a differential stage, as the stage 38,40, is determined by the time constant of the load 42/44 in the stage since the bipolar transistors can be considered as ideal current sources. The loads can be considered as pure RC-loads with the resistance of the PMOS-transistors 42 and 44 and the capacitance consisting of the parasitic capacitances of the latter and of the transistors 38,40, and connection network plus loads following thereafter. The capacitive loads are constant whereas the resistance can be controlled via the control voltage V_{RC} of the PMOS-transistors 42,44. The swing of the output signal at 48 is determined by the current from the current source, i.e. the NMOS-transistor 34 and the load resistance 42/44. The current can be controlled via the control voltage V_{RE} on the NMOS-transistor 34.

The circuit shown in Figure 1 is a basic building block, which can be varied in many ways in order to provide the

desired function. What always is common is however the collector resistances and the current sources and their location toward positive and negative supply voltage, respectively.

5 Figure 2 illustrates how logic circuitry can be built with the aid of the parts, which are shown in the basic logic stage 4 in Figure 1. Parts corresponding to those in Figure 1 have been provided with the same reference designations. More particularly, what is shown as an example is the design of an
10 exclusive-OR-gate which is bandwidth controlled in accordance with the invention. To the right of the detailed circuit the established symbol thereof is shown. As the gate circuit is of a conventional type known per se, it is not necessary to describe its design in detail here.

15 Shortly, however, the circuit is of a differential type, i.e. each logic input, designated A and B, respectively, of the operational stage 37, is associated at each input with two differentially operating signal conductors INP and INN. A logic high level, or 1, on input A implies that INP on A is
20 more positive than INN on A. A logic low level, or 0, on A implies that INN is more positive than INP. The same reasoning is of course also valid for the differential output of the operational stage, designated X.

The function of the gate can be described as follows:

25 If the status of the inputs is regarded as a vector (A,B), the vectors (0,0) and (1,1) shall result in a logic 0 on the output, and the vectors (0,1) and (1,0) shall result in a logic 1 on the output.

30 Considering the transistor circuit diagram, the vector (0,1) makes the current from 34 to be conducted through Q1 and Q4, this resulting in UTN being low and UTP being high. The vector (0,0) makes the current to be conducted through Q2 and Q6, which makes UTP to be low and UTN to be high, and so on. The transistors Q7 and Q8 and the current drains NM2 and

NM3 have the purpose to achieve a voltage shift in order for the logic levels to work practically. By means of the circuit solution shown, the drive currents through the transistors Q7 and Q8 will have the same magnitude as the one through the logic circuitry.

In the control circuit system according to the invention, e.g. according to Figure 1 or 2, or the further embodiment described below, the reference stage and the controlled logic circuitry/delay circuit are preferably arranged on the same substrate, here silicon, in order to make different parameters, temperature etc. equal for the reference stage and logic circuitry, respectively. It is also possible to use several reference stages more locally and distribute currents to these and by this avoid problems, if any, resulting from temperature gradients.

Loads and current sources in the controlled logic circuitry or the delay circuit can exhibit various sizes, i.e. be scaled up and down or in different directions in relation to the ones of the reference stage, but the control of the parameters of these is always maintained.

In Figure 3 there is illustrated the use of a reference stage of the type described above in association with a delay circuit in the form of a current controlled oscillator. In the Figure the reference stage is designated 50, said stage creating the two reference quantities V_{RC} and V_{RE} with the aid of a reference current I_{ref} . The oscillator can be designed in a way known per se with two delay stages 52 and 54, which both will receive the said reference quantities.

The delay stages 52, 54, in their simplest form, can be designed as the stage 4 in Figure 1. In general, however, they can include several such basic logic stages depending on the application. The input of the stages 52, 54 indicates that the stages are bandwidth controlled by a reference coming from a reference stage.

In Figure 4 there is illustrated the use of two reference stages of the type described above for bandwidth control of mixed logic circuitry. The reference circuits are here designated 60 and 62, respectively, and generate each the reference quantities V_{RC} and V_{RE} with the aid of a respective reference current I_{ref1} and I_{ref2} , respectively. These reference quantities are supplied to five logic stages in the way shown, said stages being only shown symbolically as two D-flipflops 64 and 66, one exclusive-OR gate 68, one OR-gate 70 and one AND-gate 72, respectively. The gate 68 can be designed as described above with reference to Figure 2.

The stages 52, 54, 64-72 have in common that they can each be defined as comprising, in accordance with the invention, and in the same way as in Figures 1 and 2, although not shown in Figures 3 and 4:

at least one operational circuit, at least one operational current source for supplying a first drive current to said operational stage, and at least one operational load, and a number of first controllable current source and load components of said operational current source and said operational load for admitting control of the magnitude of said first drive current and of said operational load, respectively.

Furthermore, the reference stages 50, 60 and 62 have in common that they can each be defined, also in accordance with the invention, and in the same way as shown in Figures 1 and 2, although not shown in Figures 3 and 4, as comprising an image circuit of the operational stage with

a reference current source for supplying a second drive current for said reference stage, and a reference load, said reference current source and said reference load comprising a number of second controllable current source and load components for admitting control of the magnitude of said second drive current and of said reference load,

respectively, and being essentially identical to said first current source and load components, respectively, said reference stage also including

5 an input stage connected for receiving an adjustable reference parameter and for controlling, by means of said reference parameter, current supply from said reference current source and said operational current source to said second and first controllable load components,

10 a comparison and control circuit connected for comparing the magnitude of said reference load with a load reference and for controlling an operational parameter of said reference load components and operational load components so as to keep the relationship between said reference load and said load reference the same irrespective of the magnitude of
15 the current through said reference load, and thereby keep the operational point of said operational stage constant for various drive currents in the latter.

Claims

1. A control circuit system for controlling one or more parameters in a circuit with

5 at least one operational stage (4;52,54;64-72), particularly a differential stage, in the form of delay stage or a logic stage, said operational stage including

at least one operational circuit (37), at least one operational current source (34) for supplying a first drive current to said operational stage, and at least one
10 operational load (41),

said control circuit system being characterized by also comprising

a number of first controllable current source and load
15 components (34 and 42,44, respectively) of said operational current source (34) and said operational load (41) for admitting control of the magnitude of said first drive current and of said operational load, respectively,

at least one reference stage (2;50;60,62) comprising
20 essentially an image circuit (10,20) of said operational stage (4) with

a reference current source (10) for supplying a second drive current for said reference stage, and a reference load (20), said reference current source and said reference load
25 comprising a number of second controllable current source and load components (10 and 20, respectively) for admitting control of the magnitude of said second drive current and of said reference load, respectively, and being essentially identical to said first current source and load components, respectively, said reference stage also including

30 an input stage connected for receiving an adjustable reference parameter (I_{ref}) and for controlling, by means of said reference parameter, current supply from said reference current source (10) and said operational current source (34)

to said second and first controllable load components (42,44;20), respectively,

5 a comparison and control circuit (22-28) connected for comparing the magnitude of said reference load (20) with a load reference (V_r) and for controlling an operational parameter of said reference load components (20) and operational load components (42,44) so as to keep the relationship between said reference load (20) and said load reference (V_r) the same irrespective of the magnitude of the
10 current through said reference load, and thereby keep the operational point of said operational stage constant for various drive currents in the latter.

2. A control circuit system according to claim 1, characterized by said operational parameter of said reference
15 load components and operational load components being the voltage drop over the respective components.

3. A control circuit system according to claim 1 or 2, characterized by said reference parameter being a reference current (I_{ref}) and said input stage including a transistor
20 component (8) connected for throughflow of said reference current, and by said reference and operational current sources including each an essentially identical transistor component (10 and 34, respectively)), the control electrodes of which being connected to a voltage outlet (12) of said
25 transistor component (8) of said input stage.

4. A control circuit system according to claim 3, characterized by said transistor components (8 and 10) of said input stage and said reference current source being interconnected in a current image circuit.

30 5. A control circuit system according to any of the above claims, characterized by said load components (20 and 42,44, respectively) of said reference stage (2) and said operational stage (4) are transistor components, having control electrodes to which a voltage output from said

comparison and control circuit (22-28) is connected.

5 6. A control circuit system according to claim 5, characterized by said comparison and control circuit including an operational amplifier (22) having a first input (24) connected for sensing the voltage over said load transistor component (20) of said reference stage and a second input connected for sensing a fixed reference voltage (V_R) constituting said load reference.

10 7. A control circuit system according to claim 3 or 4, characterized by said transistor components of said reference and operational current sources being NMOS-transistors (20 and 34).

15 8. A control circuit system according to claim 7 and any of the claims 5 or 6, characterized by said transistor components of said reference and operational loads being PMOS-transistors (20 and 42,44).

9. A control circuit system according to any of the preceding claims, characterized by comprising a plurality of reference stages (60,62).

20 10. A control circuit system according to any of the preceding claims, characterized in that loads (41) and current sources (34) included in said operational stage (4) have another size than corresponding loads and current sources included in said reference stage (2).

25 11. A control circuit system according to any of the preceding claims, characterized by said operational stage (4) including different combinations and numbers of operational circuits (37), operational current source (34) and operational load (41).

30 12. A control circuit system according to any of the preceding claims, characterized by said controlling one or more parameters including optimization, and said parameters include power and/or bandwidth and/or delay.

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Fig. 1

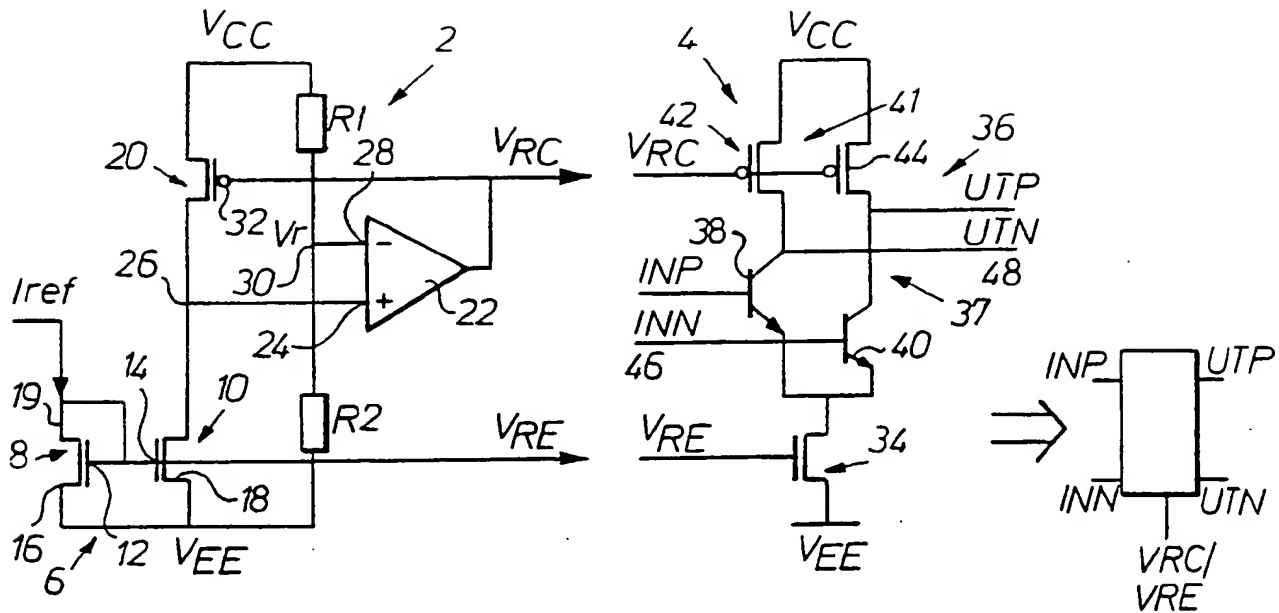


Fig. 2

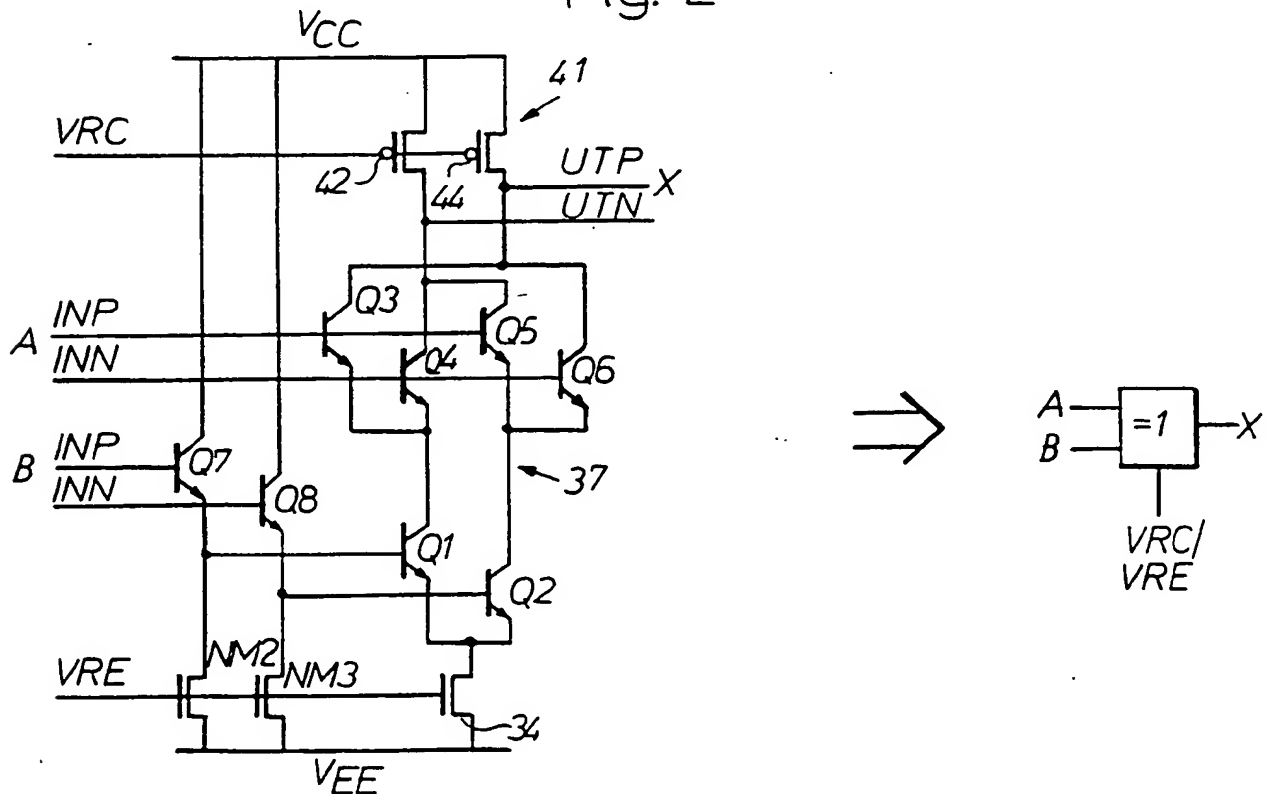


Fig. 3

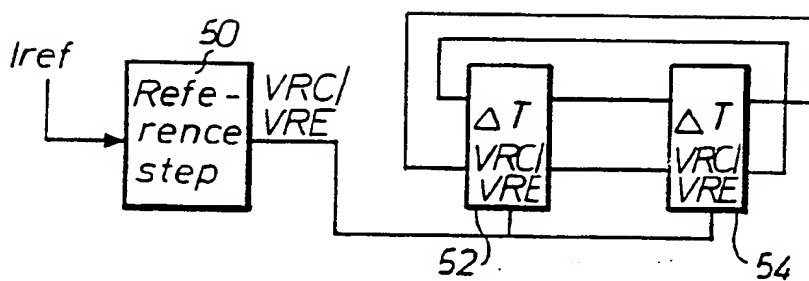
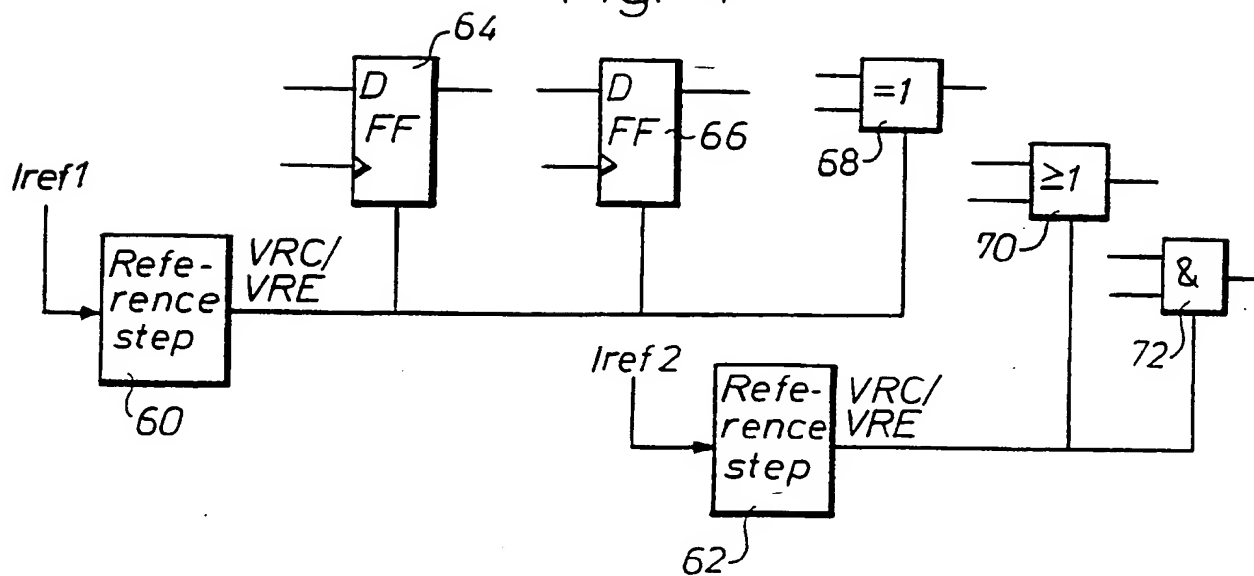


Fig. 4



INTERNATIONAL SEARCH REPORT

International application No.

PCT/SE 93/00520

A. CLASSIFICATION OF SUBJECT MATTER

IPC5: H03K 19/0175, H03K 19/003, H03K 17/00, H03K 17/687, H03K 19/094
 According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4791318 (STEPHEN R. LEWIS ET AL), 13 December 1988 (13.12.88), column 3, line 27 - column 4, line 55, figure 2, abstract --	1-12
A	US, A, 4410813 (CHARLES E. BARKER ET AL), 18 October 1983 (18.10.83), figures 1-2, abstract --	1-12
A	US, A, 4435652 (EMSLEY H. STEVENS), 6 March 1984 (06.03.84), figures 1-3, abstract -- -----	1-12

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INTERNATIONAL SEARCH REPORT

Information on patent family members

26/08/93

International application No.

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Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US-A-	4791318	13/12/88	NONE		
US-A-	4410813	18/10/83	CA-A-	1167116	08/05/84
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